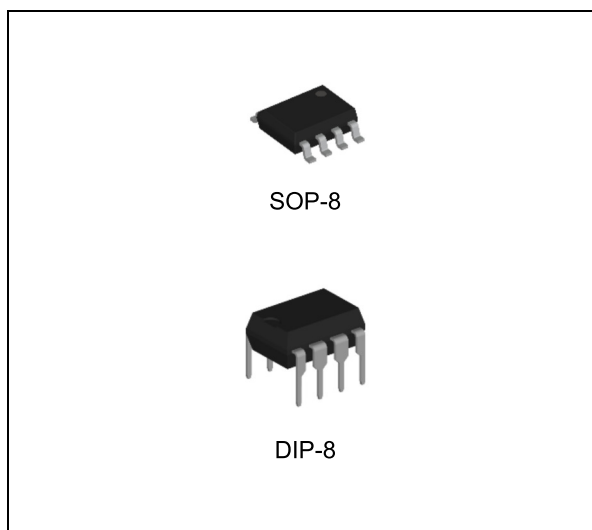


FEATURES

- Output Switch Current In Excess of 1.5A
- 2% Reference Accuracy
- Low Quiescent Current : 2.5mA(Typ.)
- Operating From 3V to 40V
- Frequency Operation to 100KHz
- Active Current Limiting
- MC34063AG is Halogen Free Products

APPLICATION

- Battery Chargers
- NICs / Switches / Hubs
- ADSL Modems
- Negative Voltage Power Supplies

**ORDERING INFORMATION**

Device	Package
MC34063AGD	SOP-8
MC34063AGN	DIP-8

DESCRIPTION

The MC34063AG series is a monolithic control circuit delivering the main functions for DC-DC voltage converting. The device contains an internal temperature compensated reference, comparator, duty cycle controlled oscillator with an active current limit circuit driver and high current output switch.

Output voltage is adjustable through two external resistors with a 2% reference accuracy.

Employing a minimum number of external components the MC34063AG devices series is designed for Step-Down, Step-Up and Voltage-Inverting applications.

ABSOLUTE MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Power Supply Voltage	V_{CC}	-	40	V
Comparator Input Voltage Range	V_{IR}	-0.3	40	V
Switch Collector Voltage	V_{SWC}		40	V
Switch Emitter Voltage($V_{SWC}=40V$)	V_{SWE}		40	V
Switch Collector to Emitter Voltage	V_{CE}		40	V
Driver Collector Voltage	V_{dc}	-	40	V
Driver Collector Current (Note 2)	I_{dc}	-	100	mA
Switch Current	I_{SW}	-	1.5	A

ABSOLUTE MAXIMUM RATINGS (Continued)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Junction Temperature Range	T_J	-40	150	°C
Storage Temperature Range	T_{STG}	-65	150	°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(*) This value depends from thermal design of PCB on which the device is mounted.

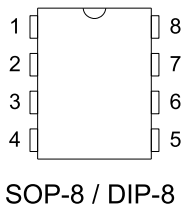
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{CC}	3	40	V
Operating Junction Temperature	T_J	-40	125	°C
Operating Ambient Temperature	T_A	-40	125	°C

ORDERING INFORMATION

Package	Order No.	Description	Supplied As	Status
SOP-8	MC34063AGD	1.5A, 100kHz	Tape & Reel	Active
DIP-8	MC34063AGN	1.5A, 100kHz	Tube	Active

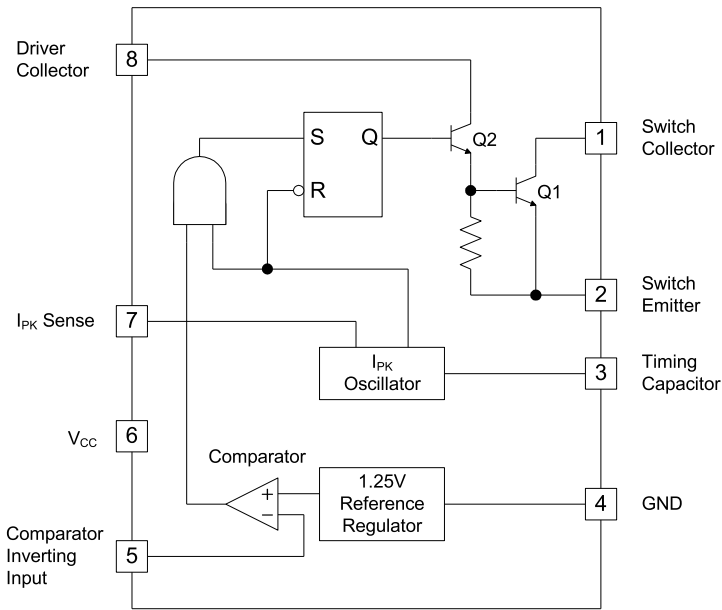
PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	DIP-8 PKG	
	Name	Function
1	Switch Collector	Internal switch transistor collector
2	Switch Emitter	Internal switch transistor emitter
3	Timing Capacitor	Timing Capacitor to control the switching frequency
4	GND	Ground pin for all internal circuits
5	Comparator Inverting Input	Inverting input pin for internal comparator
6	V _{CC}	Voltage supply
7	I _{PK} Sense	Peak Current Sense Input by monitoring the voltage drop across an external I sense resistor to limit the peak current through the switch
8	Driver Collector	Voltage driver collector

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS(Refer to the test circuits, $V_{CC}=5V$, $T_A=T_{LOW}$ to T_{HIGH} , unless otherwise specified, see note 2)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
OSCILLATOR						
F_{OSC}	Frequency	$V_{PIN5}=0V$, $C_T=1nF$, $T_A=25^\circ C$	24	33	42	KHz
I_{CHG}	Charge Current	$V_{CC}=5$ to $40V$, $T_A=25^\circ C$	24	35	42	μA
I_{DISCHG}	Discharge Current	$V_{CC}=5$ to $40V$, $T_A=25^\circ C$	140	220	260	μA
I_{DISCHG}/I_{CHG}	Discharge to Charge Current Ratio	Pin 7 = V_{CC} , $T_A=25^\circ C$	5.2	6.5	7.5	
$V_{IPK(SENSE)}$	Current Limit Sense Voltage	$I_{CHG}=I_{DISCHG}$, $T_A=25^\circ C$	250	300	350	mV
OUTPUT SWITCH						
$V_{CE(SAT)}$	Saturation Voltage, Darlington connection	$I_{SW}=1A$, Pins 1,8 connected		1.0	1.3	V
$V_{CE(SAT)}$	Saturation Voltage	$I_{SW}=1A$, $R_{PIN8}=82\Omega$ to V_{CC} , Forced $\beta \sim 20$		0.45	0.7	V
h_{FE}	DC Current Gain	$I_{SW}=1A$, $V_{CE}=5V$, $T_A=25^\circ C$	50	75		
$I_{C(OFF)}$	Collector Off-State Current	$V_{CE}=40V$		1.0	100	μA
COMPARATOR						
V_{TH}	Threshold Voltage	$T_A=25^\circ C$	1.225	1.25	1.275	V
		$T_A=T_{LOW}$ to T_{HIGH}	1.21		1.29	V
REG_{LINE}	Threshold Voltage Line Regulation	$V_{CC}=3$ to $40V$		1.4	5	mV
I_{IB}	Input Bias Current	$V_{IN}=0V$		-20	-400	nA
TOTAL DEVICE						
I_{CC}	Supply Current	$V_{CC}=5$ to $40V$, $C_T=1nF$ Pin7 = V_{CC} , $V_{PIN5}>V_{TH}$, Pin2=GND Remaining pins open		1.4	4	mA

Note 1. Maximum package power dissipation limit must be observed.

Note 2. $T_{LOW} = -40^\circ C$, $T_{HIGH} = +125^\circ C$

Note 3. If Darlington configuration is not used, care must be taken to avoid deep saturation of output switch.

The resulting switch-off time may be adversely affected.

In a Darlington configuration the following output driver condition is suggested:

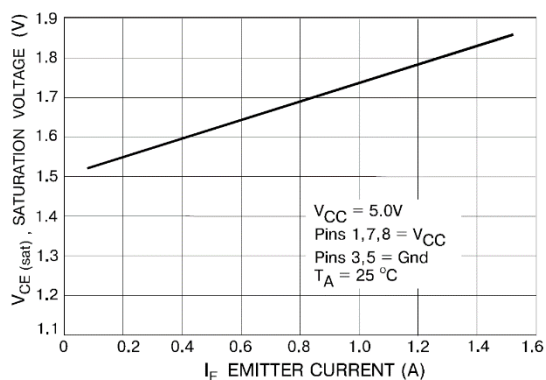
$$\text{Forced } \beta \text{ of output switch : } \frac{I_{C(OUTPUT)}}{I_{C(DRIVER)} - 7.0mA^*} \geq 10$$

* Currentless due to a built in $1K\Omega$ anti-leakage resistor

TYPICAL ELECTRICAL CHARACTERISTICS

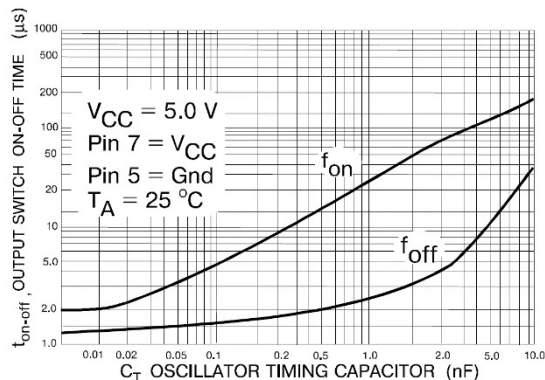
Emitter Follower Configuration Output

Saturation Voltage vs. Emitter Current



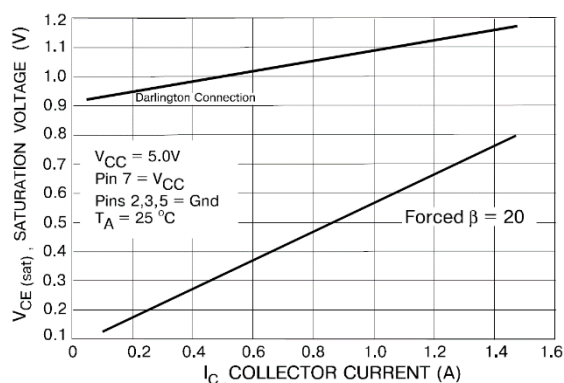
Output Switch ON-OFF Time

vs. Oscillator Timing Capacitor



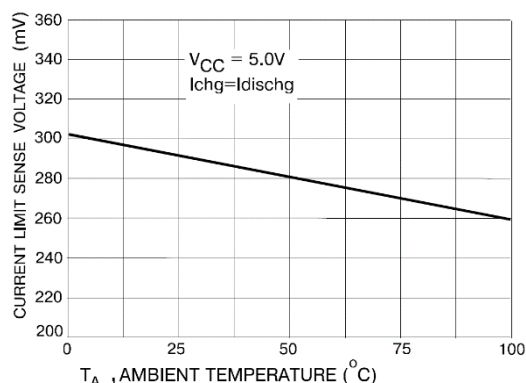
Common Emitter Configuration Output Switch

Saturation Voltage vs. Collector Current

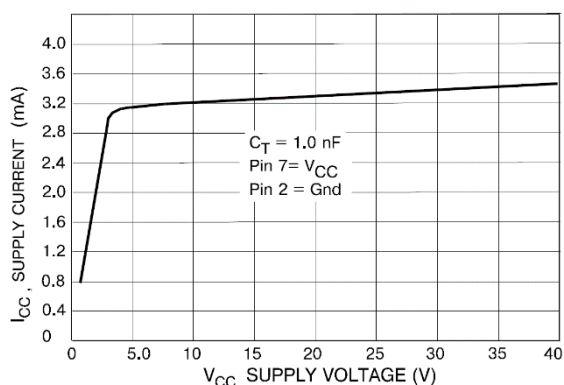


Current Limit Sense Voltage (V_{IPK})

vs. Temperature

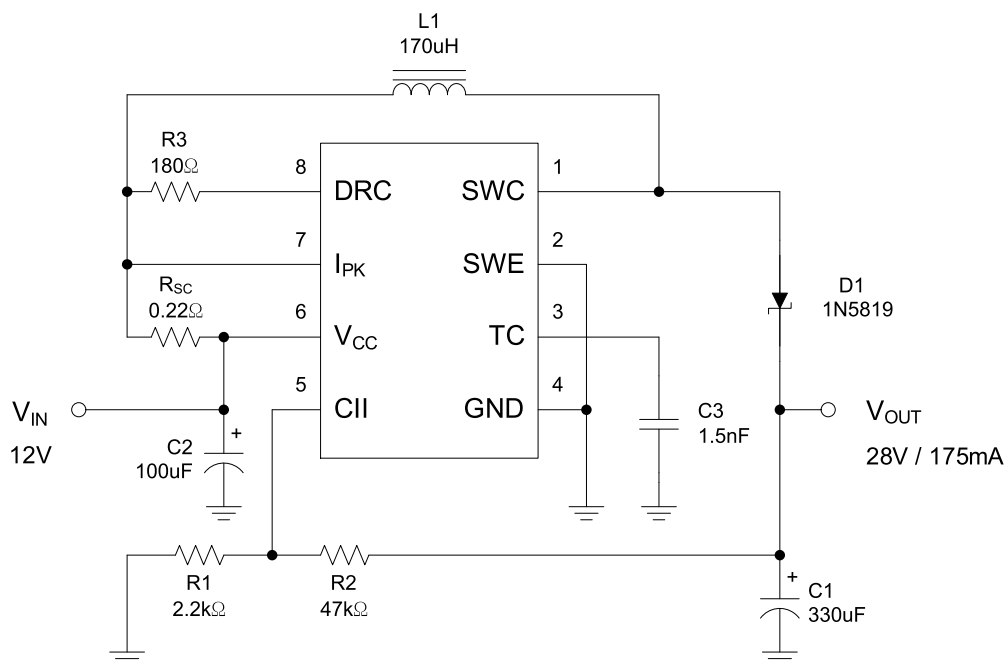


Standby supply current vs. Supply voltage

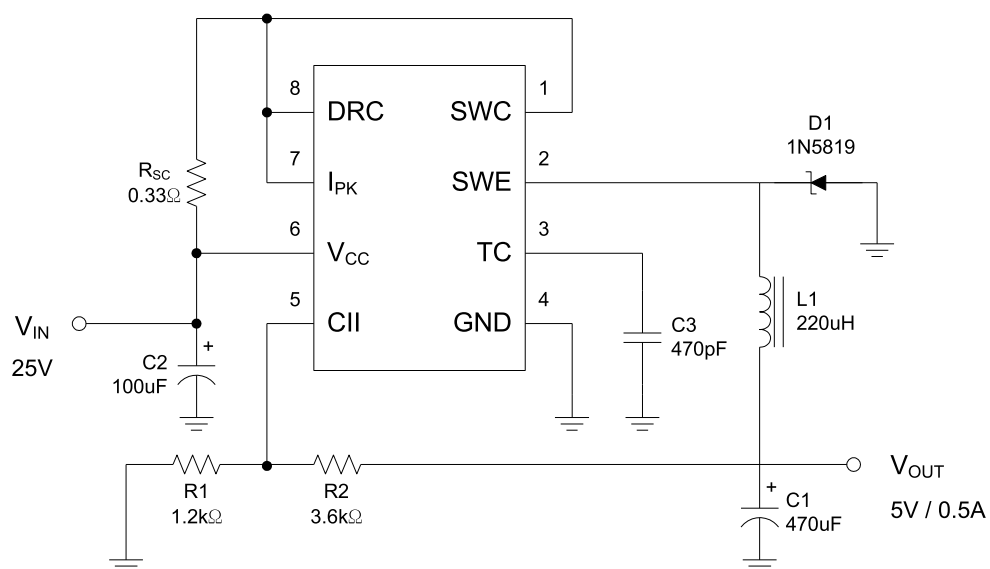


TYPICAL APPLICATION CIRCUIT

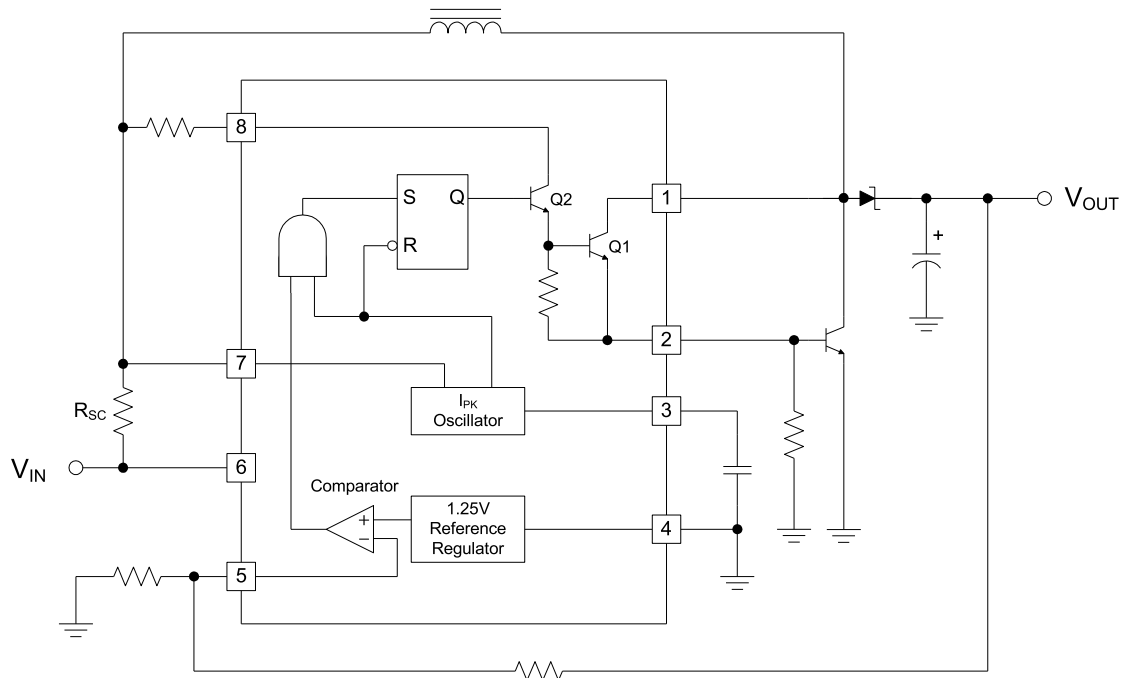
Step-Up Converter



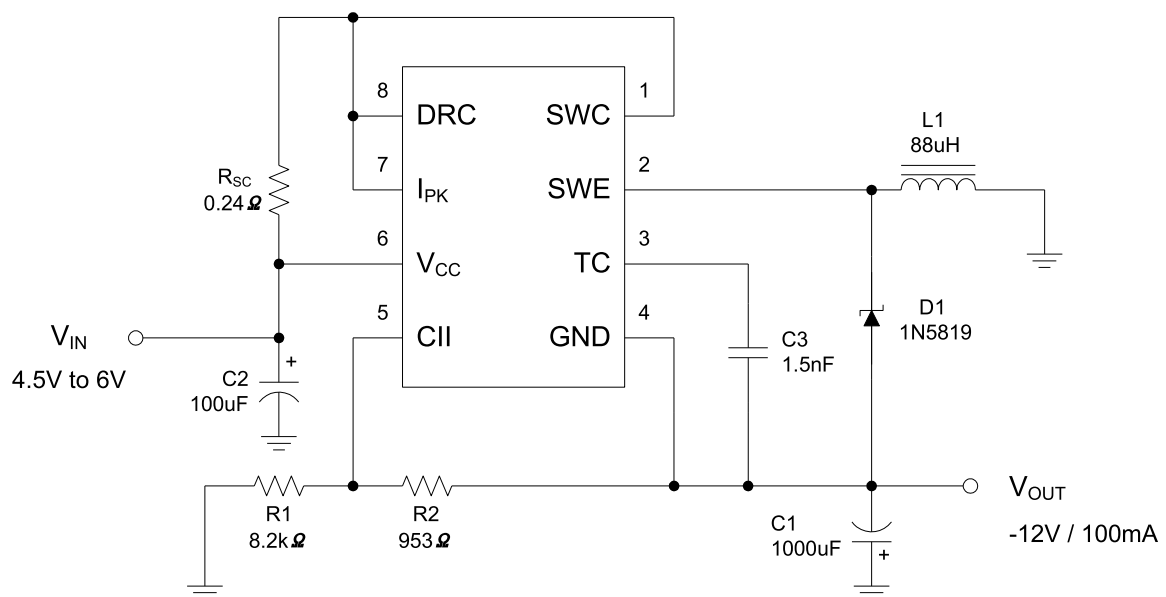
Step-Down Converter



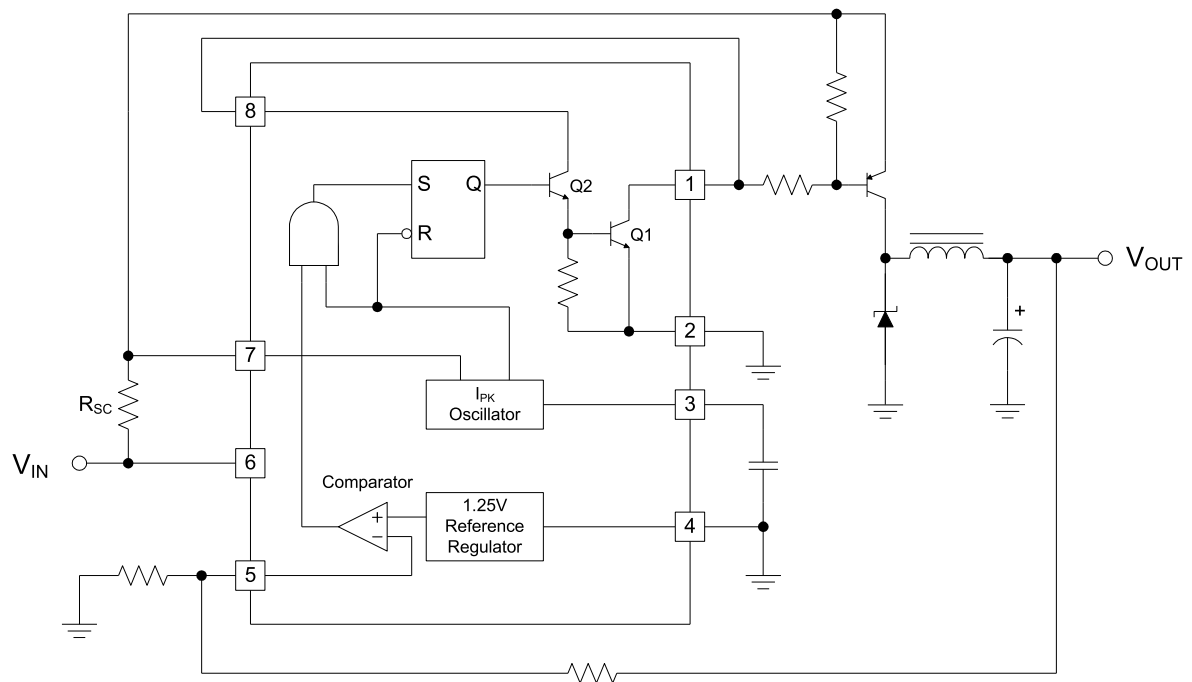
Step-Up with External NPN Switch



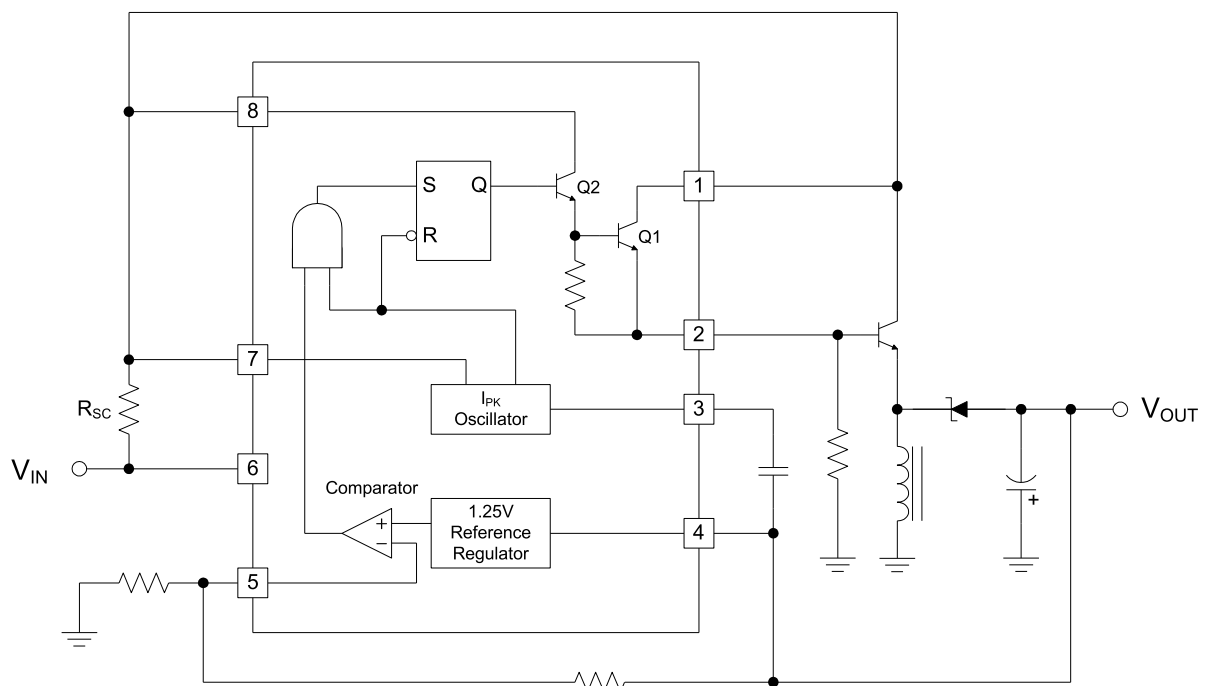
Voltage Inverting Converter



Step-Down with External PNP Switch



Voltage Inverting with External NPN Switch



DESIGN FORMULA TABLE

CALCULATION	STEP-UP	STEP-DOWN	VOLTAGE-INVERTING
t_{on} / t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_F}{V_{in} + V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.0 \times 10^{-5} \times t_{on}$	$4.0 \times 10^{-5} \times t_{on}$	$4.0 \times 10^{-5} \times t_{on}$
$I_{pk(switch)}$	$2 \times I_{out(max)} \times \left(\frac{t_{on}}{t_{off}} + 1\right)$	$2 \times I_{out(max)}$	$2 \times I_{out(max)} \times \left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{SC}	$\frac{0.3}{I_{pk(Switch)}}$	$\frac{0.3}{I_{pk(Switch)}}$	$\frac{0.3}{I_{pk(Switch)}}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(Switch)}}\right) \times t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(Switch)}}\right) \times t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(Switch)}}\right) \times t_{on(max)}$
C_O	$9 \times \frac{I_{out} \times t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)} \times (t_{on} + t_{off})}{8 \times V_{ripple(pp)}}$	$9 \times \frac{I_{out} \times t_{on}}{V_{ripple(pp)}}$

V_{SAT} - Saturation voltage of the output switch.

V_F - Forward voltage drop of the output rectifier.

V_{in} - Nominal input voltage.

V_{out} - Desired output voltage, $V_{out} = 1.25(1+R2/R1)$

f_{min} - Minimum desired output switching frequency at the selected values of V_{in} and I_{out} .

$V_{ripple(p-p)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

REVISION NOTICE

The description in this datasheet can be revised without any notice to describe its electrical characteristic properly.