FEATURES

- Input Voltage Range: 1.1V to 3.6V
- Output Voltage Range: 0.6 V to 1.8 V
- Ultra Low Dropout Voltage
- Low Quiescent Current
- Excellent Line and Load Regulation
- Guaranteed Output Current of 2.0A
- V_{OUT} Power OK Signal
- Programmable Soft-Start
- Logic Controlled Shutdown Option
- Over-Temperature/Over-Current Protection
- -40℃ to 125℃ Junction Temperature Range

APPLICATION

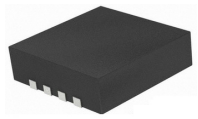
- Motherboards and Graphic Cards
- Microprocessor and Chipset Power Supplies
- Peripheral Cards
- Low Voltage Digital ICs
- High Efficiency Linear Regulators
- SMPS Post Regulators

DESCRIPTION

The TJ2132 is a 2.0A high performance ultra low-dropout linear regulator ideal for powering core voltages of low-power microprocessors. The TJ2132 implements a dual supply configuration allowing for very low output impedance. The TJ2132 requires a bias input supply and a main input supply, allowing for ultra-low input voltages on the main supply rail. The input supply operates from 1.1V to 3.6V and the bias supply requires between 2.7V and 5.5V for proper operation. The output voltage is adjustable from 0.6V to 1.8V using an external resistor divider. The Soft-Start reduces inrush current of the load capacitors and minimizes stress on the input power source during start-up. The TJ2132 delivers high current and ultra-low-dropout output voltage as low as 0.6V for applications where V_{OUT} is very close to V_{IN}. The TJ2132 is developed on a CMOS technology which allows low quiescent current operation independent of output current. This technology also allows the TJ2132 to operate under extremely low dropout conditions.

SOP8-PP

DFN 3x3-8L



ORDERING INFORMATION

Device	Package
TJ2132GDP	SOP8-PP
TJ2132GQ	DFN 3x3-8L

OPERATING RATINGS

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Recommend Operating Input Voltage	V_{IN}	1.1	3.6	V
Recommend Operating Bias Voltage	V_{BIAS}	V_{OUT}+2.1	5.5	V
Recommend Enable Input Voltage	V_{EN}	0	5.5	V
Recommend Output Voltage Range	V_{OUT}	0.6	1.8	V
Operating Junction Temperature Range	T_{JOPR}	-40	125	℃
Package Thermal Resistance*	$\Theta_{JA\text{-}SOP8\text{-}PP}$	68		℃/W

* Calculated from package in sill air, mounted to 2.6mm X 3.5mm(minimum foot print) 2 layer PCB without thermal vias per JESD51 standards.

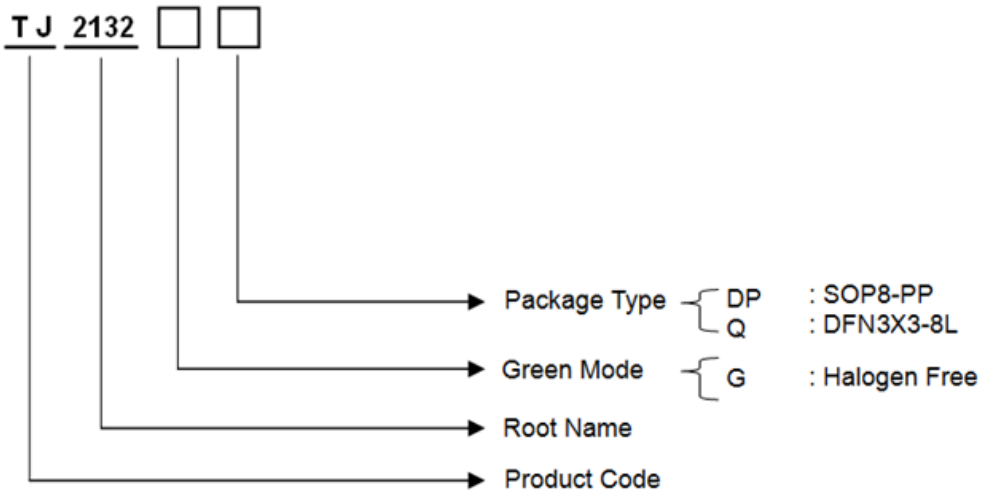
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Lead Temperature (Soldering, 5 sec)	T_{SOL}	-	260	℃
Storage Temperature Range	T_{STG}	-65	150	℃
Input Voltage	$V_{IN,ABS}$	0	4.0	V
Bias Voltage	$V_{BIAS,ABS}$	0	6.0	V
Enable Input Voltage	$V_{EN,ABS}$	0	6.0	V
Allowable Power Dissipation(Note 1)	$P_{D,max}$	-	Internally Limited	W

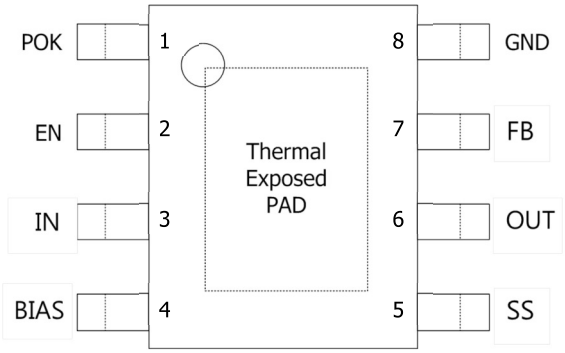
Note 1. See the 'Maximum Output Current Capability' on page 12~14.

ORDERING INFORMATION

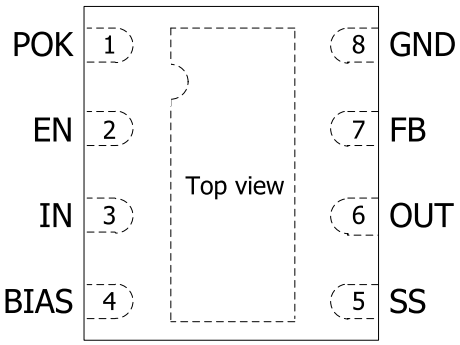
Package	Order No.	Description	Package Marking	Compliance	Supplied As
SOP8-PP	TJ2132GDP	2.0A, Enable, Adjustable, Power OK, Soft start	TJ2132G	RoHS, Halogen Free	Reel
DFN 3x3-8L	TJ2132GQ	2.0A, Enable, Adjustable, Power OK, Soft start	2132	RoHS, Halogen Free	Reel



PIN CONFIGURATION



SOP8-PP

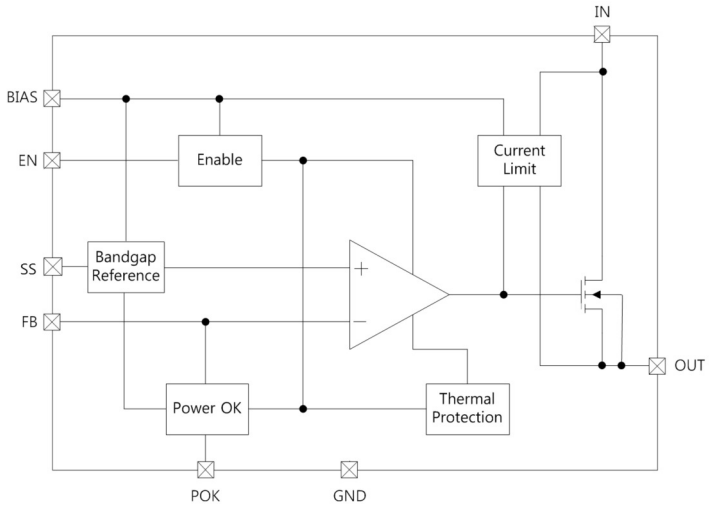


DFN 3x3-8L

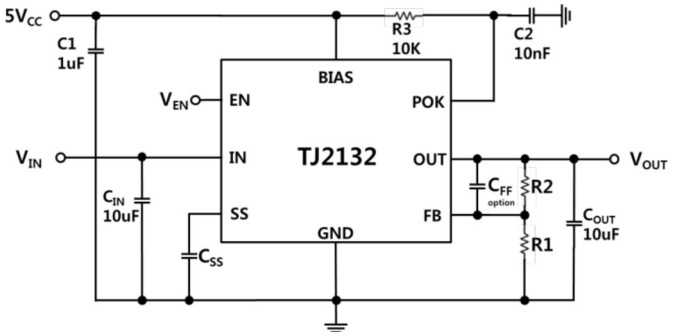
PIN DESCRIPTION

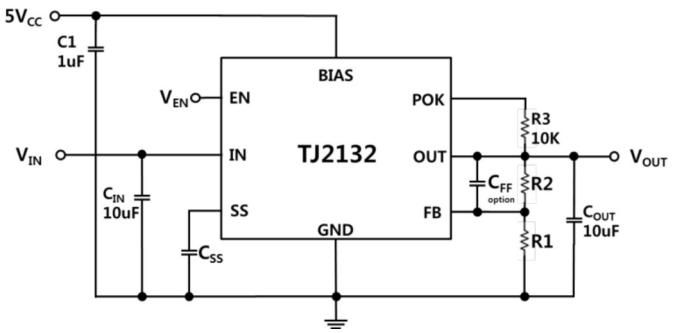
Pin No.	Pin Name	Pin Function
1	POK	Power OK Indication. This pin is an Open-drain output and is set high impedance once V_{OUT} reaches 92% of its rating voltage.
2	EN	Enable Input. Pulling this pin below 0.4V turns the regulator off. Do not float.
3	IN	Power Input. This pin is the drain input to the power device that supply current to output pin.
4	BIAS	Supply Input for Internal Circuit. Input Bias Voltage for powering all circuitry on the regulator except the output power TR.
5	SS	Soft-Start Pin. Connect a capacitor between this pin and the ground to determine the soft-start time. If soft-start is not needed, the SS pin can be left floating. (Do not connect to ground directly.)
6	OUT	Power Output. This pin is power output of the device.
7	FB	Feedback Voltage. A resistor divider from the output to GND is used to set the regulation voltage as V_{OUT}= 0.6V x (1+R2/R1)
8	GND	Ground
-	Thermal Exposed PAD	Connect to Ground.

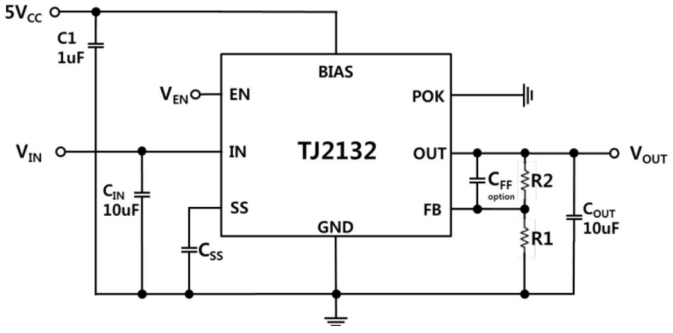
BLOCK DIAGRAM



TYPICAL APPLICATION







ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{BIAS} = 5V, V_{IN} = $V_{O(NOM)}$ + 0.5V, V_{EN}=V_{BIAS}, I_L = 10 mA, T_J=25℃.

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Input Voltage		V_{IN}	V_{OUT}=V_{REF}	1.1	-	3.6	V
Bias Input Voltage		V_{BIAS}	V_{OUT}=V_{REF}	2.7	-	5.5	V
			V_{OUT}>V_{REF}	V_{OUT}+2.1	-	5.5	V
Output Voltage		V_{OUT}		0.6	-	1.8	V
Reference Voltage		V_{REF}	V_{BIAS}=V_{EN}=5.0V, I_{OUT}=10mA, V_{OUT}=V_{REF}	0.588	0.6	0.612	V
V_{IN} Line Regulation(Note 2)		$\Delta V_{LINE(IN)}$	V_{OUT}+0.5V<V_{IN}<3.6V, I_{OUT}=10mA	-	0.02	0.10	%/V
V_{BIAS} Line Regulation(Note 3)		$\Delta V_{LINE(BIAS)}$	V_{OUT}+2.1V<V_{BIAS}<5.5V, I_{OUT}=10mA, V_{OUT}=V_{REF}	-	0.02	0.10	%/V
Load Regulation(Note 4)		ΔV_{LOAD}	10mA < I_L <2A, V_{IN}=1.4V, V_{BIAS}= V_{EN}=5.0V, V_{OUT}=V_{REF}	-	0.05	0.35	%/A
Dropout Voltage		V_{DROP}	I_L = 0.5A, V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	65	100	mV
			I_L = 1.0A, V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	130	180	
			I_L = 2.0A, V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	250	380	
Ground Pin Current(Note 5)		I_{GND1}	I_L = 10mA	-	0.1	0.5	mA
			I_L = 2.0 A	-	0.1	0.5	mA
		I_{GND2}	V_{EN} < 0.4 V, POK=open (Note 6)	-	0.1	1.0	uA
Enable Threshold	Logic High	V_{IH}	Output=High	1.5	-	-	V
	Logic Low	V_{IL}	Output=Low	-	-	0.4	V
EN Input Current		I_{EN}	V_{EN}=V_{BIAS}=5.0V	-	-	0.5	uA
FB Power OK Threshold		V_{POKTH}	V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	92	-	%
Power OK Hysteresis		V_{POKHYS}	V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	7	-	%
OCP Threshold Level		I_{OCP}	V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	3.5	-	A
Thermal Shutdown Temperature		T_{SD}		-	165	-	℃
Thermal Shutdown Hysteresis		ΔT_{SD}		-	20	-	℃

Note 2. Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage.

Note 3. Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the bias line voltage.

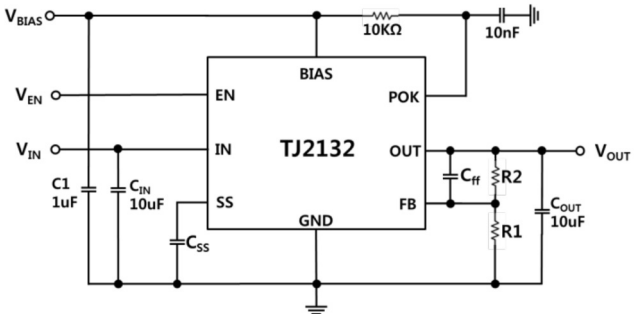
Note 4. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. Regulation is measured at constant junction temperature by using a 10ms current pulse. Devices are tested for load regulation in the load range from 10mA to 2.0A

Note 5. I_{GND} = I_{BIAS} + (I_{IN} – I_{OUT}). The total current drawn from the supply is the sum of the load current plus the ground current.

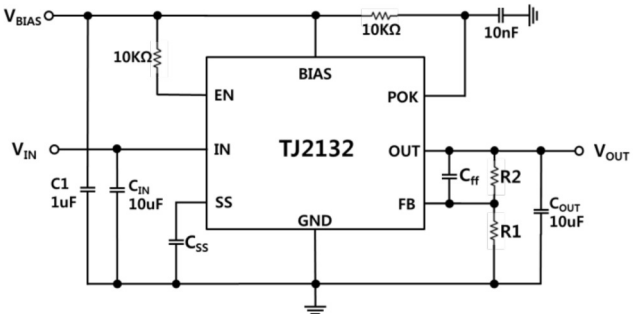
Note 6. When POK pin is applied to V_{BIAS} through the resistor R3, I_{GND2} should be added to the bias current (V_{BIAS} - V_{POK}) / R3.

TYPICAL OPERATING CHARACTERISTICS

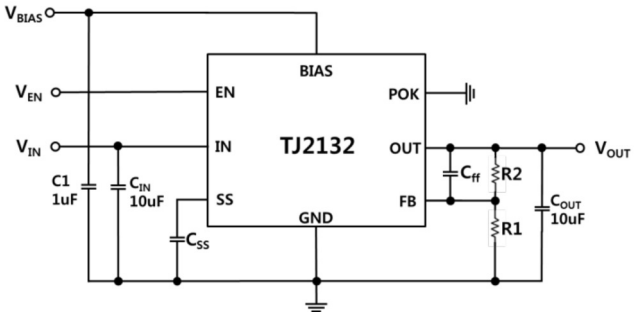
- TEST Circuit



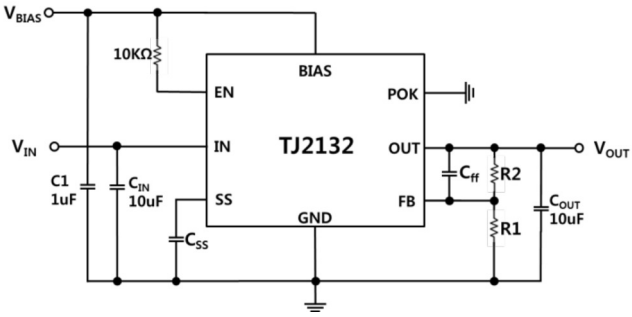
Circuit #01



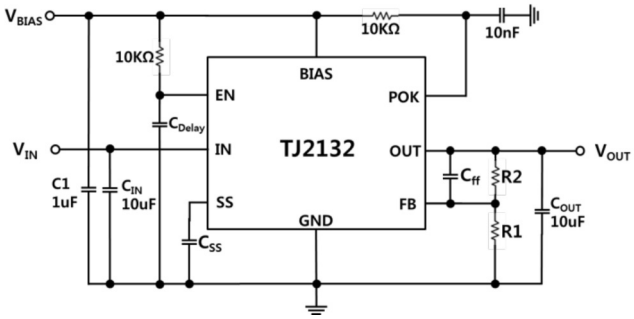
Circuit #02



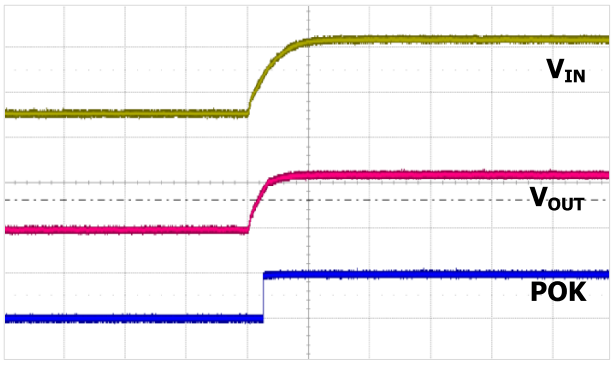
Circuit #03



Circuit #04



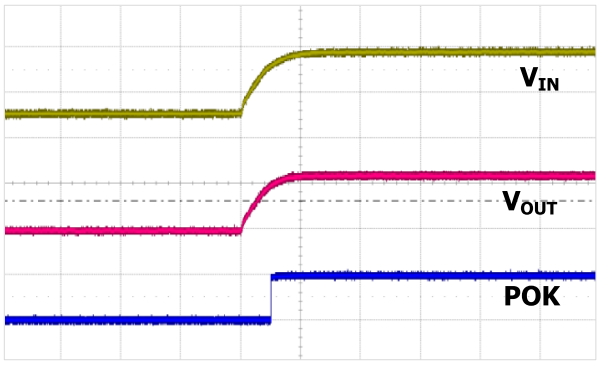
Circuit #05



- V_{IN}: 1V/div, V_{OUT}: 1V/div, POK: 5V/div, 500us/div

Start up @ I_{OUT}=10mA, Circuit #1

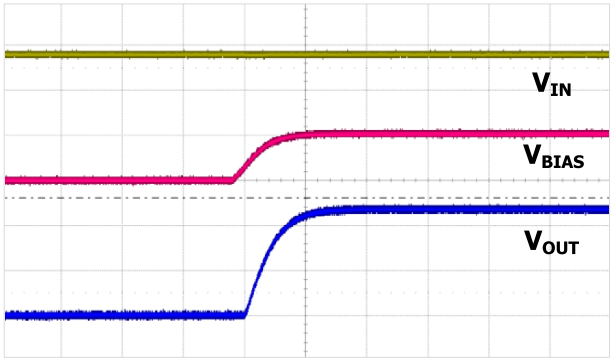
(C_{ff}=10nF, C_{SS}=470pF, R1=R2=10kΩ, V_{EN}=V_{BIAS}=5.0V)



- V_{IN}: 1V/div, V_{OUT}: 1V/div, POK: 5V/div, 500us/div

Start up @ I_{OUT}=2A, Circuit #1

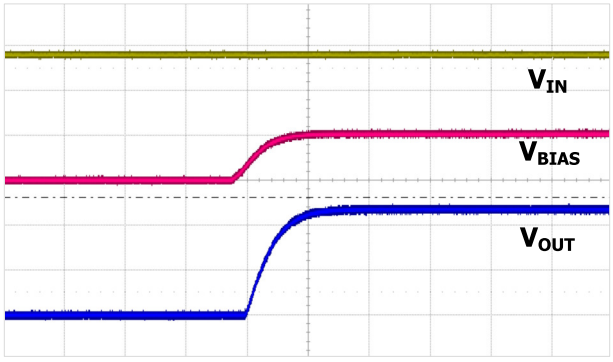
(C_{ff}=10nF, C_{SS}=470pF, R1=R2=10kΩ, V_{EN}=V_{BIAS}=5.0V)



- V_{IN}: 2V/div, V_{BIAS}: 5V/div, V_{OUT}: 500mV/div, 500us/div

Start up @ I_{OUT}=10mA, Circuit #2

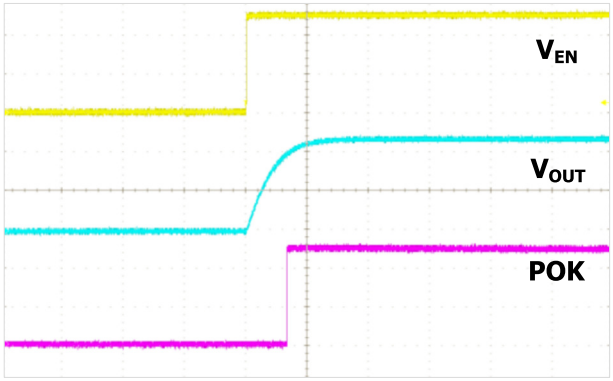
(C_{ff}=10nF, C_{SS}=470pF, R1=R2=10kΩ, V_{IN}=1.7V, V_{EN}=5.0V)



- V_{IN}: 2V/div, V_{BIAS}: 5V/div, V_{OUT}: 500mV/div, 500us/div

Start up @ I_{OUT}=2A, Circuit #2

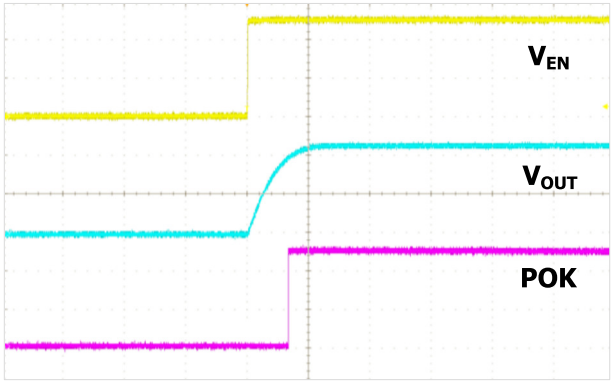
(C_{ff}=10nF, C_{SS}=470pF, R1=R2=10kΩ, V_{IN}=1.7V, V_{EN}=5.0V)



- V_{EN}: 2V/div, V_{OUT}: 500mV/div, POK: 2V/div, 500us/div

Start up @ I_{OUT}=10mA, Circuit #1

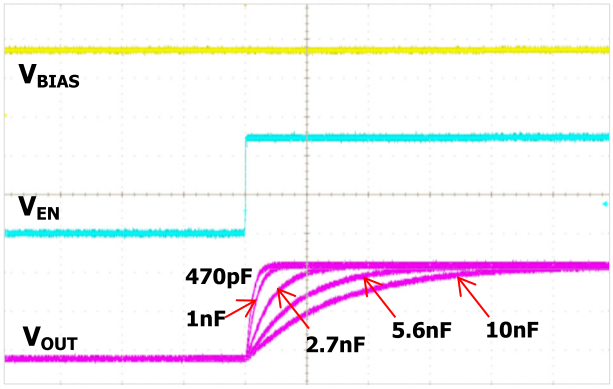
(C_{ff}=10nF, C_{SS}=470pF, R1=R2=10kΩ, V_{IN}=1.7V, V_{BIAS}=5.0V)



- V_{EN}: 2V/div, V_{OUT}: 500mV/div, POK: 2V/div, 500us/div

Start up @ I_{OUT}=2A, Circuit #1

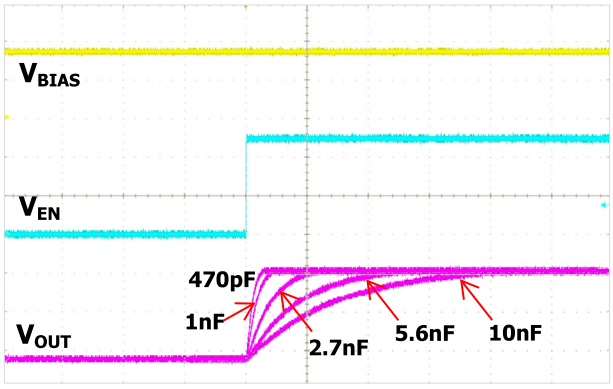
(C_{ff}=10nF, C_{SS}=470pF, R1=R2=10kΩ, V_{IN}=1.7V, V_{BIAS}=5.0V)



- V_{BIAS}: 3V/div, V_{EN}: 2V/div, V_{OUT}: 500mV/div, 2ms/div

Start up @ I_{OUT}=10mA, Circuit #1

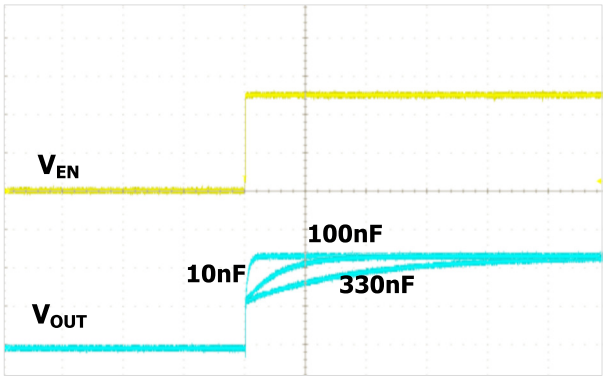
(C_{SS} is varied, C_{ff}=10nF, R1=R2=10kΩ, V_{IN}=1.7V, V_{EN}=V_{BIAS}=5.0V)



- V_{BIAS}: 3V/div, V_{EN}: 2V/div, V_{OUT}: 500mV/div, 2ms/div

Start up @ I_{OUT}=2A, Circuit #1

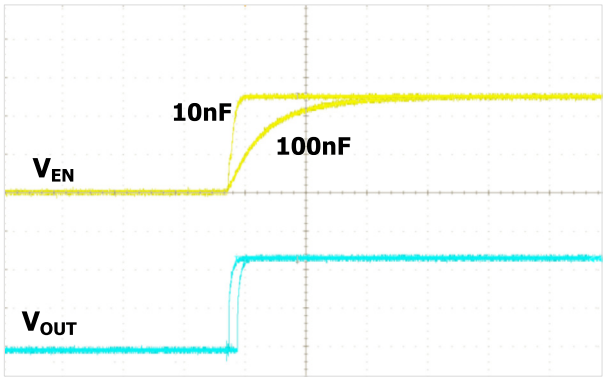
(CSS is varied, C_{ff}=10nF, R1=R2=10kΩ, V_{IN}=1.7V, V_{EN}=V_{BIAS}=5.0V)



- V_{EN}: 2V/div, V_{OUT}: 500mV/div, 1ms/div

Start up @ I_{OUT}=10mA, Circuit #1

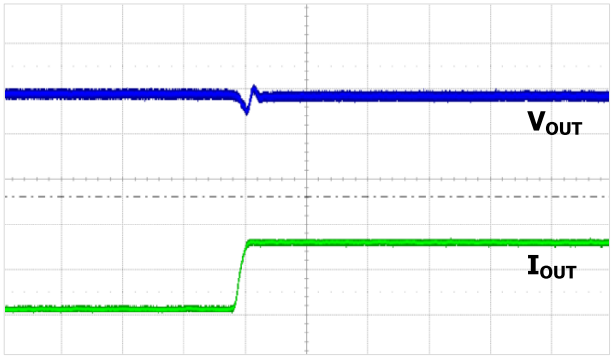
(C_{ff} is varied, C_{SS}=open, R1=R2=10kΩ, V_{IN}=1.7V, V_{BIAS}=5.0V)



- V_{EN}: 2V/div, V_{OUT}: 500V/div, 2ms/div

Start up @ I_{OUT}=10mA, Circuit #5

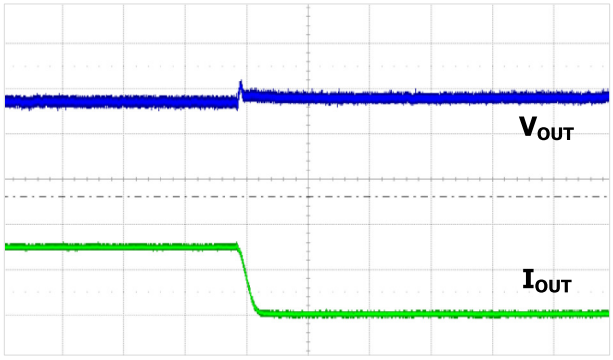
(C_{delay} is varied, C_{SS}=open, R1=R2=10kΩ, V_{IN}=1.7V, V_{BIAS}=5.0V)



- V_{OUT}: 100mV/div, I_{OUT}: 1A/div, 200us/div

Load Transient Response

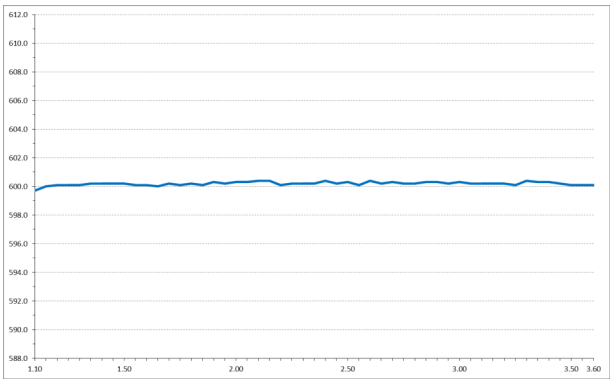
(C_{ff}=10nF, C_{SS}=470pF, R1=R2=10kΩ, V_{IN}=1.7V, V_{EN}=V_{BIAS}=5.0V)



- V_{OUT}: 100mV/div, I_{OUT}: 1A/div, 200us/div

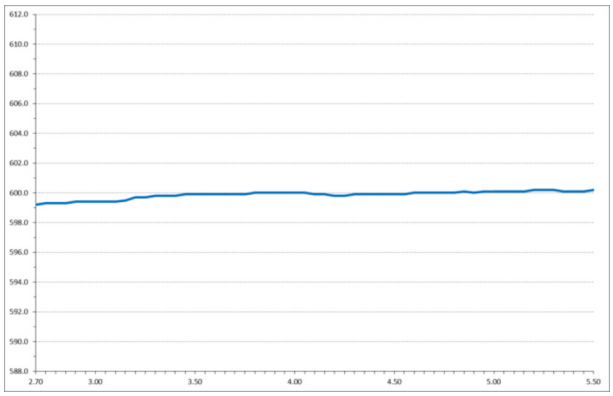
Load Transient Response

(C_{ff}=10nF, C_{SS}=470pF, R1=R2=10kΩ, V_{IN}=1.7V, V_{EN}=V_{BIAS}=5.0V)



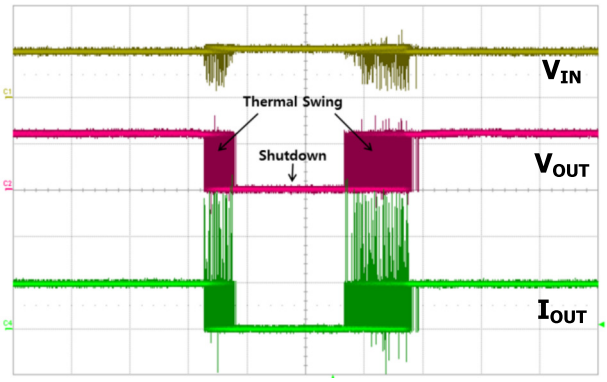
- x-axis: V_{IN} [V], y-axis: V_{OUT} [mV]

V_{OUT} vs. V_{IN} @ V_{BIAS}=5.5V



- x-axis: V_{BIAS} [V], y-axis: V_{OUT} [mV]

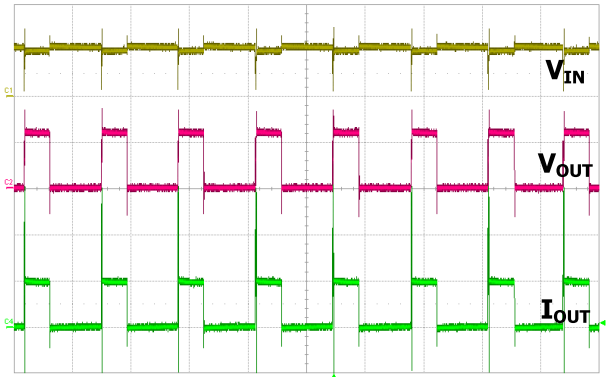
V_{OUT} vs. V_{BIAS} @ V_{IN}=3.6V



- V_{IN}: 2.0V/div, V_{OUT}: 1.0V/div, I_{OUT}: 2A/div, 5.0s/div

Thermal Shutdown & Recovery

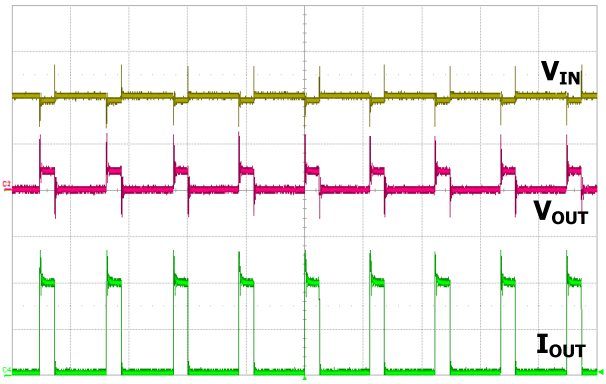
(C_{SS}=470pF, R1=R2=10kΩ, V_{IN}=2.0V, V_{EN}=V_{BIAS}=5.0V)



- V_{IN}: 2.0V/div, V_{OUT}: 1.0V/div, I_{OUT}: 2A/div, 10ms/div

Thermal Swing

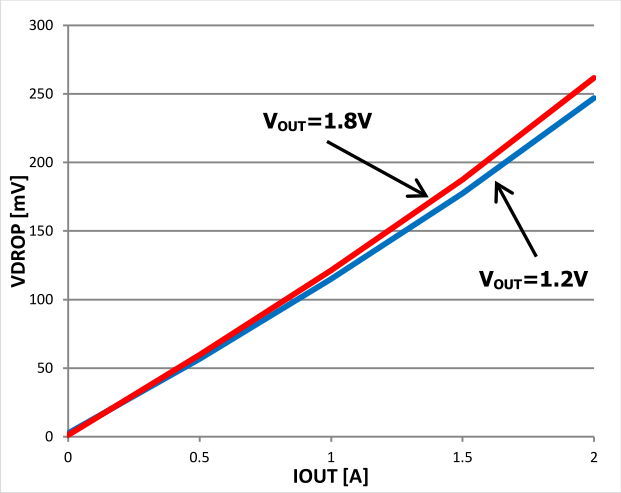
(C_{SS}=470pF, R1=R2=10kΩ, V_{IN}=2.0V, V_{EN}=V_{BIAS}=5.0V)



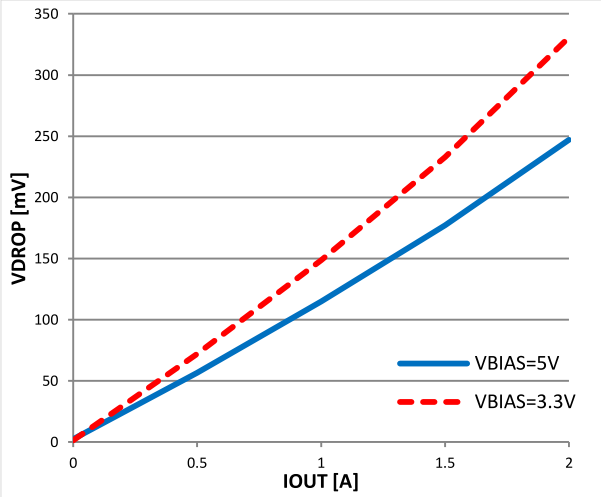
- V_{IN}: 2.0V/div, V_{OUT}: 1.0V/div, I_{OUT}: 2A/div, 1.0ms/div

Short Circuit Response

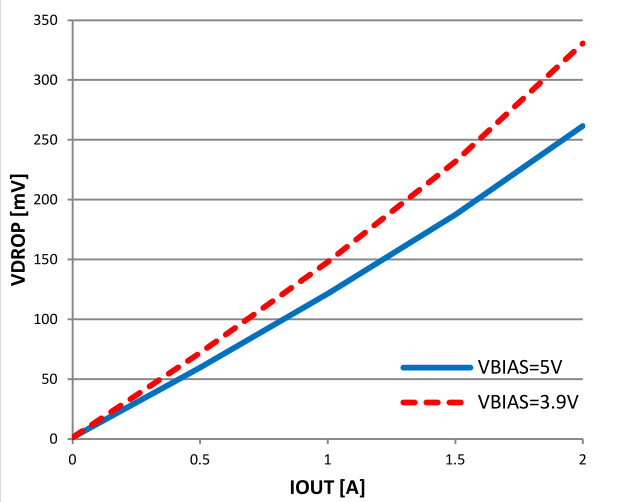
(C_{SS}=470pF, R1=10kΩ, R2=20kΩ, V_{IN}=4.0V, V_{EN}=V_{BIAS}=5.5V)



Dropout Voltage



V_{DROP} vs. V_{BIAS} @ V_{OUT}=1.2V



V_{DROP} vs. V_{BIAS} @ V_{OUT}=1.8V

APPLICATION INFORMATION

The TJ2132 is a high performance, low dropout linear regulator, designed for high current application that requires fast transient response. The TJ2132 operates from two input supply voltages, significantly reducing dropout voltage. The TJ2132 is designed so that a minimum of external component are necessary.

Bias Supply Voltage

The TJ2132 control circuitry is supplied by the BIAS pin which requires a very low bias current even at the maximum output current level. A bypass capacitor on the bias pin is recommended to improve the performance of the TJ2132 during line and load transient. A small ceramic capacitor from BIAS pin to ground reduces high frequency noise that could be injected into the control circuitry from the bias rail. In practical applications, a 1uF capacitor and smaller valued capacitors such as 0.01uF or 0.001uF in parallel with that larger capacitor may be used to decouple the bias supply. The BIAS input voltage must be 2.1V above the output voltage, with a minimum BIAS input voltage of 2.7V.

Adjustable Regulator Design

An adjustable output device has output voltage range of 0.6V to 1.8V. To obtain a desired output voltage, the following equation can be used two external resistors as presented in the typical application circuit. The resistor values are given by;

$$R_2 = R_1 \times (\frac{V_{OUT}}{0.6} - 1) \qquad (1)$$

It is suggested to use R1 values lower than 10kΩ to obtain better load transient performances. Even, higher values up to 100 kΩ are suitable.

Enable

The TJ2132 feature an active high Enable input (EN) that allows on/off control of the regulator. The enable function of TJ2132 has hysteresis characteristics. Pulling V_{EN} lower than 0.4V disables the chip. Pulling V_{EN} higher than 1.5V enables the output voltage.

Supply Power Sequencing

In common applications where the power on transient of V_{IN} and V_{BIAS} voltages are not particularly fast (Tr > 100us), no power sequencing is required. Where voltage transient input is very fast(Tr<100us), it is recommended to have the V_{IN} voltage present before or, at least, at the same time as the V_{BIAS} voltage in order to avoid over voltage spikes during the power on transient.

Output Capacitors

The TJ2132 requires an of output capacitance to maintain stability. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The TJ2132 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor which value is at least 10uF on the TJ2132 output ensures stability. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. A minimum ceramic capacitor over than 10uF should be very closely placed to the output voltage pin of the TJ2132. When applying an output capacitor that has big capacitance, the soft start time using soft start capacitor at SS pin should be carefully adjusted to avoid any in-rush current problem.

Input Capacitor

A large bulk capacitance over than 10uF should be closely placed to the input supply pin of the TJ2132 to ensure that the input supply voltage does not sag. Also a minimum of 10uF ceramic capacitor is

recommended to be placed directly next to the IN pin. It allows for the device being some distance from any bulk capacitor on the rail. Additionally, input droop due to load transients is reduced, improving load transient response. Additional capacitance may be added if required by the application.

Soft Start Time

The TJ2132 has an internal current source that charges an external slow start capacitor to implement a slow start time. Equation 2 and Table 1 shows how to select a slow start capacitor based on an expected slow start time. The R is 302kΩ, V_O is 0.6V and i(t) is 40nA. Adjustment of soft start time using SS pin capacitor is help to suppress unexpected abnormal in-rush current that can cause device failure.

$$T_{SS}(\mathrm{s}) = -\mathrm{R}C_{SS} \times \ln\frac{i(t)R}{V_O} \quad (2)$$

Table 1. Capacitor Values for the soft-start time

C_{SS}	Calculated Soft-Start Time	Measured Soft-Start Time
470pF	0.56ms	0.64ms
1nF	1.18ms	1.23ms
2.7nF	3.18ms	3.44ms
5.6nF	6.6ms	7.1ms
10nF	11.8ms	12.0ms

Decoupling (Bypass) Capacitor

In very electrically noisy environments, it is recommended that additional ceramic capacitors be placed from VIN to GND. The use of multiple lower value ceramic capacitors in parallel with output capacitor also allows to achieve better transient performance and stability if required by the application. (See Fig.1)

Feed-Forward Capacitor

To get the higher PSRR than the inherent performance of TJ2132, it is recommended that additional ceramic feed-forward capacitor be placed from OUT pin to FB pin. The capacitance of feed-forward capacitor with range of 10pF to 1uF allows to achieve better PSRR performance when required by the application. (See Fig.1)

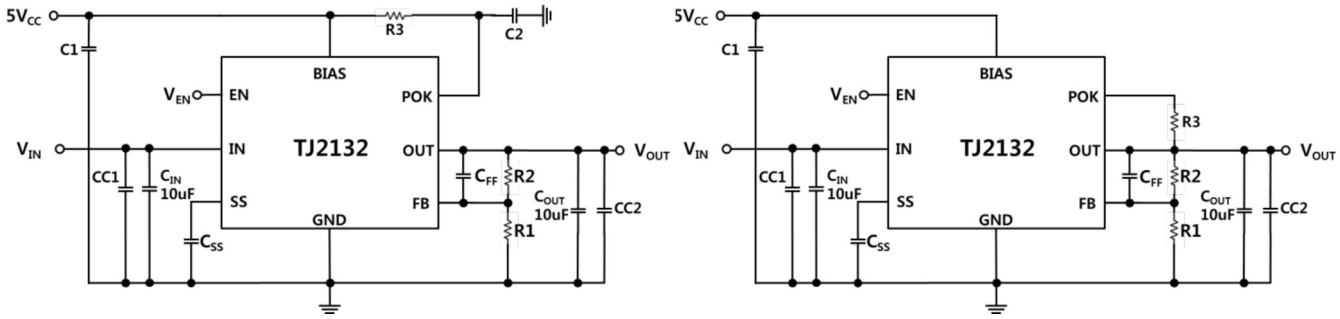


Fig.1 Application with Decoupling & Feed-Forward Capacitor

Maximum Output Current Capability

The TJ2132 can deliver a continuous current of 2A over the full operating junction temperature range.

However, the output current is limited by the restriction of power dissipation which differs from packages. A heat sink may be required depending on the maximum power dissipation and maximum ambient temperature of application. With respect to the applied package, the maximum output current of 2A may be still undeliverable due to the restriction of the power dissipation of TJ2132. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.
The temperatures over the device are given by:

$$T_C = T_A + P_D \text{ X } \theta_{CA}$$
$$T_J = T_C + P_D \text{ X } \theta_{JC}$$
$$T_J = T_A + P_D \text{ X } \theta_{JA}$$

where T_J is the junction temperature, T_C is the case temperature, T_A is the ambient temperature, P_D is the total power dissipation of the device, θ_{CA} is the thermal resistance of case-to-ambient, θ_{JC} is the thermal resistance of junction-to-case, and θ_{JA} is the thermal resistance of junction to ambient.

The total power dissipation of the device is given by:

$$P_D = P_{IN} - P_{OUT} = \{(V_{IN} \text{ X } I_{IN}) + (V_{BIAS} \text{ X } I_{BIAS})\} - (V_{OUT} \text{ X } I_{OUT})$$

where I_{GND} is the operating ground current of the device which is specified at the Electrical Characteristics. The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

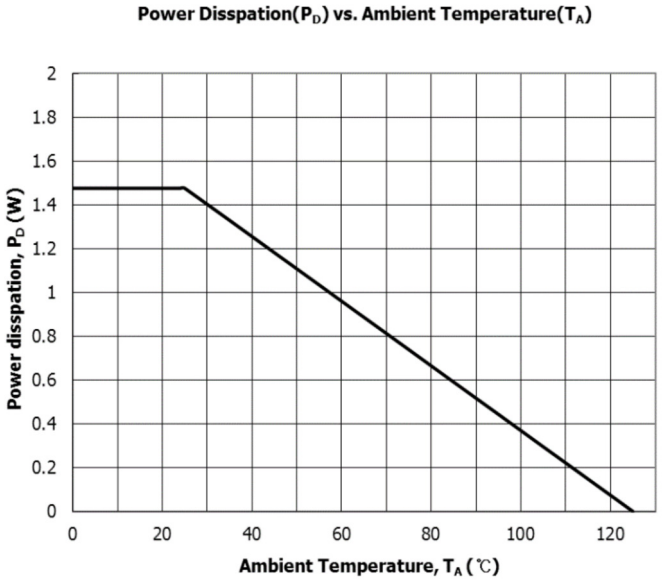
$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

The maximum allowable value for junction-to-ambient thermal resistance, θ_{JA}, can be calculated using the formula:

$$\Theta_{JA} = T_{Rmax} / P_D$$

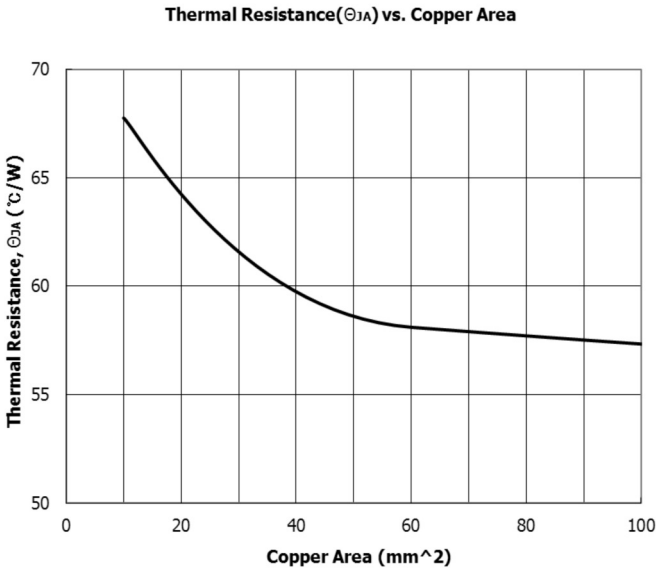
TJ2132 is available in SOP8-PP packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow.

If proper cooling solution such as heat sink, copper plane area, or air flow is applied, the maximum allowable power dissipation could be increased. However, if the ambient temperature is increased, the allowable power dissipation would be decreased.



The graph above is valid for the thermal impedance specified in the Absolute Maximum Ratings section on page 1.

The θ_{JA} could be decreased with respect to the copper plane area. So, the specification of maximum power dissipation for an application is fixed, the proper plane area could be estimated by following graphs. Wider copper plane area leads lower θ_{JA}.



The maximum allowable power dissipation is also influenced by the ambient temperature. With the θ_{JA}-Copper plane area relationship, the maximum allowable power dissipation could be evaluated with respect to the ambient temperature. As shown in graph, the higher copper plane area leads θ_{JA}. And the higher ambient temperature leads lower maximum allowable power dissipation.

REVISION NOTICE

The description in this datasheet is subject to change without any notice to describe its electrical characteristics properly.